CLAIM AMENDMENTS

IN THE CLAIMS

This listing of the claims will replace all prior versions, and listing, of claims in the application or previous response to office action:

1. (Original) A method in the fabrication of a silicon-germanium mesa transistor in a semiconductor process flow, particularly in a process flow designed for a bipolar integrated circuit for radio frequency applications, characterized by the steps of:

- providing a p-type doped silicon bulk substrate having an n^+-type doped surface region being a subcollector for the mesa transistor;
- depositing epitaxially thereon a silicon layer comprising n-type dopant;
- depositing epitaxially thereon a silicon layer comprising germanium and p-type dopant;
- forming in said epitaxial layers field isolation areas around, in a horizontal plane, a portion of said epitaxial layers to simultaneously define an n-type doped collector region for the mesa transistor on the subcollector; a p-type doped base region for the mesa transistor thereon; and an n-type doped collector plug on the subcollector, but separated from the n-type doped collector region and the p-type doped base region; and
- thereafter forming in said p-type doped base region an n-type doped emitter region for the mesa transistor.

2. (Original) The method as claimed in claim 1, wherein said field isolation areas are shallow trenches and said shallow trenches are formed and said n-type doped collector region; said p-type doped base region; and said n-type doped collector plug are defined simultaneously by means of a single etching step.

3. (Original) The method as claimed in claim 2, wherein etching in said single etching step is performed, in a vertical direction, at least down to said subcollector.

4. (Original) The method as claimed in claim 1, wherein said germanium and p-type dopant are added to said silicon layer in-situ during said-epitaxial deposition.

5. (Original) The method as claimed in claim 1, wherein said silicon layer comprising germanium and p-type dopant is a multilayer structure.

6. (Original) The method as claimed in claim 5, wherein said multilayer structure includes at least one intrinsic silicon layer.

7. (Original) The method as claimed in claim 6, wherein said multilayer structure includes at least one silicon-germanium layer between two intrinsic silicon layers.

8. (Original) The method as claimed in claim 1, wherein said silicon layer comprising germanium and p-type dopant is deposited by anyone of the techniques RP-CVD, UHV-CVD and MBE.

9. (Original) The method as claimed in claim 8, wherein said silicon layer comprising n-type dopant and said silicon layer comprising germanium and p-type dopant are both grown by RP-CVD in a single deposition sequence using the same deposition equipment.

10. (Original) The method as claimed in claim 1, wherein carbon is added to said silicon layer comprising germanium and p-type dopant to retard diffusion of said p-type dopant.

11. (Original) The method as claimed in claim 1, wherein the temperature during the fabrication of said silicon-germanium mesa transistor is kept below or at about 800 °C subsequent to the deposition of said silicon layer comprising germanium and p-type dopant apart from during a step of emitter activation and drive-in.

12. (Original) The method as claimed in claim 11, wherein the step of emitter activation and drive-in is performed using an RTA (Rapid Thermal Anneal) to electrically activate dopants, and to set the final doping profiles of the emitter-base junction of the SiGe mesa transistor.

13. (Original) The method as claimed in claim 11, wherein the step of emitter activation and drive-in is performed at high temperature, but during a short time of about 5-20 seconds.

14. (Original) The method as claimed in claim 12, wherein the step of emitter activation and drive-in is performed at high temperature, but during a short time of about 5-20 seconds.

15. (Original) The method as claimed in claim 1, wherein deep trenches are formed to surround, in a horizontal plane, said n-type doped collector region; said p-type doped base region; and said n-type doped collector plug for isolation of said silicon-germanium mesa transistor.

16. **(Withdrawn)** An SiGe mesa transistor comprising:

- a p-type doped silicon bulk substrate having an n^+-type doped surface region being a subcollector for the mesa transistor;
- an epitaxially silicon layer deposited theron comprising n-type dopant;
- an epitaxially silicon layer deposited theron comprising germanium and p-type dopant;
- field isolation areas around, in a horizontal plane, a portion of said epitaxial layers to simultaneously define an n-type doped collector region for the mesa transistor on the subcollector; a p-type doped base region for the mesa transistor thereon; and an n-type doped collector plug on the subcollector, but separated from the n-type doped collector region and the p-type doped base region; and
- an n-type doped emitter region in said p-type doped base region for the mesa transistor.

17. **(Withdrawn)** The transistor as claimed in claim 16, wherein said field isolation areas are shallow trenches.

18. **(Withdrawn)** The transistor as claimed in claim 16, wherein said silicon layer comprising germanium and p-type dopant is a multilayer structure.

19. **(Withdrawn)** The transistor as claimed in claim 18, wherein said multilayer structure includes at least one intrinsic silicon layer.

20. **(Withdrawn)** The transistor as claimed in claim 19, wherein said multilayer structure includes at least one silicon-germanium layer between two intrinsic silicon layers.

21. **(Withdrawn)** The transistor as claimed in claim 16, wherein said silicon layer comprising germanium and p-type dopant further comprises carbon to retard diffusion of said p-type dopant.

22. **(Withdrawn)** The transistor as claimed in claim 16, comprising deep trenches surrounding, in a horizontal plane, said n-type doped collector region; said p-type doped base region; and said n-type doped collector plug for isolation of said silicon-germanium mesa transistor.

23. **(Withdrawn)** An integrated circuit comprising at least one of the SiGe mesa transistor as claimed in claim 16.